**Experiment No. 08**

**Title: Realize 2 bit Comparator circuit using VHDL.**

**Batch: B1 Roll No.: 1914078 Experiment No.: 08**

**Aim:** Realize a 2 bit comparator circuit using VHDL **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_ \_**

**Resources needed:** VHDL, Online simulator.

**Theory:**

VHDL is stands for ‘Very High Speed Integrated circuit Hardware Description Language’. It is inherently parallel i.e. commands which responds to logic gate are executed to parallel as soon as input arrives.

**Sections of VHDL Code:**

There are 5 sections in VHDL:

* Entity
* Architecture
* Configuration
* Package
* Package body.

Entity and architecture are mandatory for a design but the others are optional.

**What is Entity?**

**Ans:** An entity is a black box with declaration of inputs and outputs. An example of an entity is given below:

entity full\_adder is

port (

a : in bit;

b : in bit;

cin: in bit;

sum : out bit;

carry : out bit

);

end full\_adder;

which defines a full adder with three input ports and two output ports.

**What is Architecture?Ans:**

An architecture statement defines the structure or description of a design and is bounded with an entity Since architecture describes what is inside an entity, it can be written in different ways by different designers. Some prefer dataflow while the others may prefer the structural method for a design. architecture full\_adder\_arch of full\_adder is

begin

sum <= a xor b xor cin;

carry <= (a and b) or (a and cin) or (b and cin);

end full\_adder\_arch;

**Types of Architecture:**

1. **Behavioural Style Architecture:**

A behavioural style specifies what a particular system does in a program like description using processes, but provides no details as to how a design is to be implemented.

1. **Structural Style Architecture:**

A structural style defines the structural implementation using componen t declarations and component instantiations. The following shows a structural description of the same FULL\_ADDER. Two types o f components are defined in this example, HALF\_ADDER and OR\_GATE.

Example:

VHDL Program for realizing NAND and NOR gates

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity nand\_nor\_top is

Port ( A1 : in STD\_LOGIC; -- NAND gate input 1

A2 : in STD\_LOGIC; -- NAND gate input 2

X1 : out STD\_LOGIC; -- NAND gate output

B1 : in STD\_LOGIC; -- NOR gate input 1

B2 : in STD\_LOGIC; -- NOR gate input 2

Y1 : out STD\_LOGIC); -- NOR gate output

end nand\_nor\_top;

architecture Behavioral of nand\_nor\_top is

begin

X1 <= A1 nand A2; -- 2 input NAND gate

Y1 <= B1 nor B2; -- 2 input NOR gate

end Behavioral;

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**Procedure**:

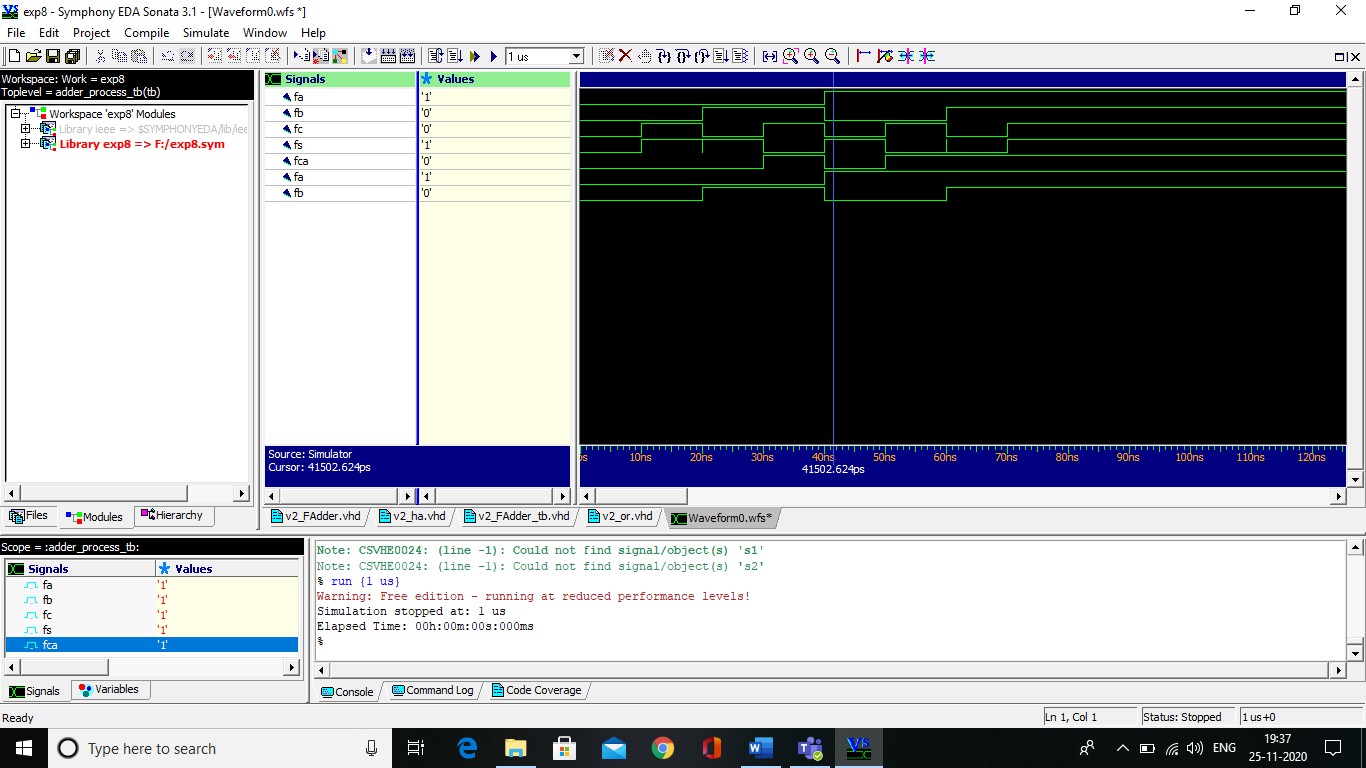
1. Complete the Theory of Experiment.
2. Write a VHDL program of 2 bit magnitude comparator.
3. Upload the write-up with VHDL code for realizing the combinational logic circuit.

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**Observations and Results:** Understand the basics of VHDL programming and its Applications.

**Output:**

The following waveform was obtained for the given code for the adder process.



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**Outcomes:**

**CO4: Design basic logic circuits using VHDL.\_**

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**Conclusion:** We learnt the implementation of VHDL programming and realized a 2 bit comparator circuit using VHDL.

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of faculty in-charge with date**

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**References:**

**Books/ Journals/ Websites:**

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2. J. Bhasker Yalamanchili, ”A VHDL Primer”, Phi Learning Private Limited Third Edition
3. <https://startingelectronics.org/software/VHDL-CPLD-course/tut3-NAND-NOR-XOR-XNOR-gates/>
4. <http://allaboutfpga.com/vhdl-4-to-1-mux-multiplexer/>